What is claimed is:

1. An interleaver memory access apparatus of a CDMA system comprising:

an interleaver memory for storing code symbols to be transmitted;

a shift register unit for simultaneously receiving 18 bit code symbols from the interleaver memory and outputting it by 6 code symbols;

an index decoding unit for decoding the 6 code symbols outputted from the shift register unit and generates a Walsh index;

an address generator and control logic for controlling the access operation of the interleaver memory and the input and output operation of the shift register unit and the index coding unit; and

an orthogonal modulator for outputting 64 Walsh codes on the basis of the Walsh index outputted from the index decoding unit.

2. The apparatus of claim 1, wherein the interleaver memory simultaneously outputs the 1-row code symbols according to a row address outputted from the address generator and control logic.

3. The apparatus of claim 1, wherein the shift register unit includes two shift registers connected in series so that when one shift register performs a reading operation, the other shift register can perform a writing operation.

4. The apparatus of claim 3, wherein each shift register includes 3 storing regions.

5. The apparatus of claim 4, wherein the shift register simultaneously outputs 6 code symbols stored in each storing region according to a data select signal outputted from the address generator and control logic.

6. The apparatus of claim 1, wherein the index decoding unit includes a first through a third index decoders for sequentially receiving code symbols by 6 ones from the shift register unit and generating one Walsh index, respectively.

7. The apparatus of claim 6, wherein the first through the third index decoders are sequentially activated according to an enable signal outputted from the address generator and control logic.

8. The apparatus of claim 1, wherein the address generator and control logic repeatedly accesses to the shift register if code symbols to be transmitted are not in a full rate.

9. The apparatus of claim 8, wherein the address generator and control logic accesses the shift register by one time in case of the half rate, repeatedly accesses to the shift register by three times in case of a quarter rate, and repeatedly accesses to the shift register by seven times in case of an eight rate.

10. An interleaver memory access method of a CDMA system comprising the steps of:

storing code symbols to be transmitted in the interleaver memory;

reading 1-row code symbols stored in the interleaver memory by using a row address signal and outputting them to the shift register unit;

repeatedly accessing the first code symbols stored in the shift register unit according to the transfer rate of the code symbols; and

decoding the 6 code symbols outputted from the shift register unit and generating one Walsh index.

11. The method of claim 10, wherein the interleaver memory writes symbol codes according to a row and a column addresses and reads symbol codes according to a row address.

12. The method of claim 10, wherein the shift register unit includes two shift registers connected in series so that when one shift register performs a reading operation, the other shift register can perform a writing operation.

13. The apparatus of claim 10, wherein each shift register includes 3 storing regions, and each region stores 6 code symbols.

14. The apparatus of claim 10, wherein if the transfer rate of the code symbols is the full rate, the shift register is not repeatedly accessed.

15. The apparatus of claim 10, wherein the shift register is accessed by one time if the transfer rate is a half rate, repeatedly accessed by three times in case of a quarter rate, and repeatedly accessed by seven times in case of an eight

rate.